REMARKS

The applicant is grateful for the opportunity to clarify the meaning of the claims responsive to the section 112 rejections of several of the claims. The claims have been modified to clarify antecedent basis and drafting irregularities, accordingly.

It is believed that no new matter has been introduced by the amendment above, and that the modifications made are a complete response to the section 112 rejections. The main difficulty appears to be the meaning of "associated". Generally the concept in the first claim had the circuit being claimed associated with a particular mid-level cache. The claims have been modified to ensure that there is no question regarding the meaning of associated in the claims.

With regard to the substantive rejection based in section 102(e) on the Amirilli reference, and with regard to the reference to other art, it is not understood how these references apply since all of the claims rely on a side door mechanism, separate and apart from the normal data pathways for communicating directly among the mid-level caches and none of the references cited contain this feature. The mid-level caches each have a side door connected generally via a radial to each other. In Amirilli, it is fairly clear that no such pathway exists. The caches of Amirilli are connected via the normal data path (Bus 8) instead, which connects them to the main memory 18. The side door/radial communication system of the applicant's invention is a radical departure from normal data pathways in multiprocessor computer systems where normally there is a system bus through which all software locks pass. In the applicant's system there is an additional pathway, the radial, that has an either an additional set of hardware controllers or added features to a standard set of hardware controllers to make it work, and it is above and beyond the ordinary communications pathways and system buses that other multiprocessor computer systems use. See the first full paragraph at the top of applicant's page 20:

Consistent with the earlier illustrations, the first level caches (like FLC0 821/871) connect the instruction processor 870/820 to their respective SLCs. (Bus 830/870 would be equivalent to the line 103 in Fig. 1 and lines 851/801 equivalent structures to the R in Figs. 5

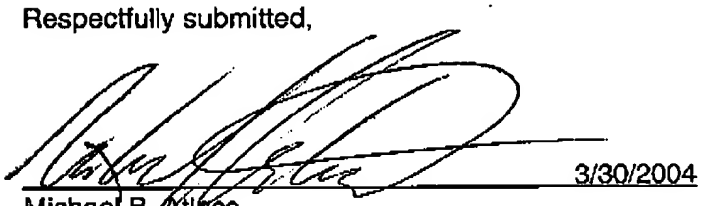
and 4). The side doors operate through controller's 802a/802b and 852a/852b, which connect to each other through a radial 801/851. The controllers also handle (although separate controllers could be used) communications with the bus 830/870 that connects the SLCs to the regular memory communications architecture.

Here, and at other locations in the application, it is detailed that there is a separate system for this CSWL inquiry communications that exists, linking the SLC's (mid-level caches) to each other via their side doors. There is nothing at all like this in any of the cited art.

It is believed that on reconsideration it will be understood that the unique arrangement of the applicant's claimed system will be found allowable, as there are no such doors nor their equivalents seen in the references, but they function as an integral limitation in all the claims.

Accordingly, applicant respectfully requests that rejection be reconsidered and that the claims be allowed and passed to issue.

Respectfully submitted,



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